AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A circuit for reducing the current density on a bus coupled to a plurality of circuits, the circuit comprising:

a folding amplifier array for a fine channel circuit of a folding analog-to-digital converter, wherein the folding amplifier array includes:

a first amplifier circuit of the plurality of circuits, wherein the first amplifier circuit is configured to provide a first output current for the bus;

a first current source circuit that is arranged to provide a first local current at an output of the first amplifier circuit such that at least a portion of the first output current is prevented from being carried on the bus;

a second amplifier circuit of the plurality of circuits, wherein the second amplifier circuit is configured to provide a second output current for the bus; and

a second current source circuit that is configured to provide a second local current at an output of the second amplifier circuit such that at least a portion of the second output current is prevented from being carried on the bus.

2. (Previously Presented) The circuit of Claim 1, wherein the folding amplifier array further includes:

a load circuit that is coupled to the bus.

3. (Original) The circuit of Claim 1, wherein

the first amplifier circuit is configured to provide the first output current to the bus in response to a first input voltage signal, and wherein

the first output current is a differential current, and the first input voltage signal is a differential voltage signal.

4. (Canceled)

5. (Canceled)

6. (Currently amended) The circuit of Claim 1[[5]], wherein the folding amplifier array further includes:

a third amplifier circuit of the plurality of circuits, wherein the third amplifier circuit is configured to provide a third output current to the bus; and

a third current source circuit that is configured to provide a third local current at an output of the third amplifier circuit.

7. (Original) The circuit of Claim 6, wherein one of the amplifier circuits in the plurality of circuits is not saturated, and each of the other amplifier circuits in the plurality of circuits is saturated.

8. (Previously Presented) The circuit of Claim 1, wherein the folding amplifier array further includes:

another bus that is coupled to another plurality of circuits;

another amplifier circuit of the other plurality of circuits, wherein the other amplifier circuit is configured to provide another output current for the other bus; and

another current source circuit that is arranged to provide another local current at an output of the other amplifier circuit such that at least a portion of the other output current is prevented from being carried on the other bus.

9. (Original) The circuit of Claim 1, wherein

the first amplifier circuit includes:

a first differential pair; and

a first tail current source that is configured to provide a first tail current, and wherein the first local current corresponds to a fraction of the first tail current.

10. (Original) The circuit of Claim 9,

wherein the fraction of the first tail current is approximately half of the first tail current.

11. (Previously Presented) A circuit, comprising:

an amplifier array circuit with a plurality of buses for a folding analog-to-digital converter circuit, wherein the amplifier array circuit is a folding amplifier array circuit for a fine channel stage of the folding analog-to-digital converter, the amplifier array circuit comprising:

a plurality of transconductance circuits;

a plurality of load circuits, wherein each of the plurality of load circuits is separately coupled to one of the plurality of buses,

wherein a first bus of the plurality of buses is coupled to a portion of the plurality of transconductance circuits;

a first current source circuit, wherein the first current source circuit is coupled to an output of a first of the portion of the plurality of transconductance circuits, and wherein the first current source circuit is arranged to provide a first local current at the output of the first transconductance circuit such that a maximum magnitude of current density is decreased on at least the first bus of the plurality of buses; and

another current source circuit that is coupled to an output of another transconductance circuit in the portion of transconductance circuits.

12. (Previously Presented) The circuit of Claim 11, wherein

one of the portion of the transconductance circuits is not saturated, and

wherein every other transconductance circuit in the portion is saturated.

13. (Canceled)

14. (Previously Presented) The circuit of Claim 11, further comprising:

a plurality of current source circuits that includes the first current source circuit,

wherein each of the plurality of transconductance circuits has an output coupled to a separate one of the plurality of current source circuits.

15. (Previously Presented) An amplifier array circuit with a plurality of buses for a folding analog-to-digital converter circuit, the amplifier array circuit comprising:

a plurality of transconductance circuits;

a plurality of load circuits, wherein each of the plurality of load circuits is separately coupled to one of the plurality of buses,

wherein a first bus of the plurality of buses is coupled to a portion of the plurality of transconductance circuits;

a first current source circuit, wherein the first current source circuit is coupled to an output of a first of the portion of the plurality of transconductance circuits, and wherein the first current source circuit is arranged to provide a first local current at the output of the first transconductance circuit such that a maximum magnitude of current density is decreased on at least the first bus of the plurality of buses; and

a plurality of current source circuits that includes the first current source circuit, wherein each of the plurality of transconductance circuits has an output coupled to a separate one of the plurality of current source circuits, wherein each of the plurality of load circuits includes a load current source, and

wherein each of the plurality of current source circuits shares a bias line in common with one of the load current sources.

16. (Previously Presented) The circuit of Claim 14, wherein

each of the plurality of transconductance circuits is configured to provide a separate transconductance current on one of the plurality of buses, and wherein

each of the plurality of current source circuits is configured to supply a separate local current such that at least a portion of the output current from each of the plurality of transconductance circuits is prevented from being carried on each of the plurality of buses.

17. (Previously Presented) The circuit of Claim 11, wherein

the first transconductance circuit is configured to provide the first transconductance current in response to a differential voltage;

the first transconductance current is differential; and wherein

the first local current is differential.

18. (Previously Presented) The circuit of Claim 11, wherein

the first transconductance circuit includes:

a first differential pair; and

a first tail current source that is configured to provide a first tail current, and wherein

the first local current corresponds to a portion of the first tail current.

19. (Original) The circuit of Claim 18,

wherein the portion of the first tail current is approximately half of the first tail current.

20. (Previously Presented) A circuit for decreasing current density on a bus coupled to a plurality of circuits, the circuit comprising:

means for folding analog-to-digital conversion, including:

means for amplifying a first input signal to provide a first current to the bus;

means for providing a first local current; and

means for canceling out at least a portion of the first current with the first local current such that a maximum magnitude of a total current on the bus is reduced.

21. (Previously Presented) A circuit for reducing the current density on a bus coupled to a plurality of circuits, the circuit comprising:

a fine channel circuit for a folded analog-to-digital converter, including a folding amplifier array, wherein the folding amplifier array includes:

a first amplifier circuit of the plurality of circuits, wherein the first amplifier circuit is configured to provide a first output current for the bus; and

a first current source circuit that is arranged to provide a first local current at an output of the first amplifier circuit such that at least a portion of the first output current is prevented from being carried on the bus.

22. (Previously Presented) The circuit of Claim 21, wherein the bus is composed of metal having substantially no resistance.

23. (Previously Presented) A circuit for reducing the current density on a bus coupled to a plurality of circuits, the circuit comprising:

a first amplifier circuit of the plurality of circuits, wherein the first amplifier circuit is configured to provide a first output current for the bus;

a first current source circuit that is arranged to provide a first local current at an output of the first amplifier circuit such that at least a portion of the first output current is prevented from being carried on the bus; and

a load circuit that is coupled to the bus, wherein the load circuit is configured to provide an output voltage such that the output voltage is substantially equal to the multiplicative product of: the bus current, and an impedance of the load circuit.

24. (Previously Presented) A circuit for reducing the current density on a bus coupled to a plurality of circuits, the circuit comprising:

a first amplifier circuit of the plurality of circuits, wherein the first amplifier circuit is configured to provide a first output current for the bus;

a first current source circuit that is arranged to provide a first local current at an output of the first amplifier circuit such that at least a portion of the first output current is prevented from being carried on the bus; and

a load circuit that is coupled to the bus, wherein the load circuit does not include averaging impedances.

25. (Previously Presented) A circuit for reducing the current density on a bus coupled to a plurality of circuits, the circuit comprising:

a first amplifier circuit of the plurality of circuits, wherein the first amplifier circuit is configured to provide a first output current for the bus;

a first current source circuit that is arranged to provide a first local current at an output of the first amplifier circuit such that at least a portion of the first output current is prevented from being carried on the bus; and

a load circuit that is coupled to the bus, wherein the load circuit is coupled to a supply voltage.

26. (Previously Presented) A circuit for reducing the current density on a bus coupled to a plurality of circuits, the circuit comprising:

a first amplifier circuit of the plurality of circuits, wherein the first amplifier circuit has at least an output that is connected to the bus, and wherein the first amplifier circuit is configured to provide a first output current at the output of the first amplifier circuit;

a first current source circuit having at least an output, wherein the output of the first current source circuit is connected to the bus, and wherein the first current source circuit is arranged to provide a first local current at an output of the first current source circuit such that at least a portion of the first output current is prevented from being carried on the bus; and

a second amplifier circuit of the plurality of circuits, wherein the second amplifier circuit has at least an output that is connected to the bus, and wherein the second amplifier circuit is configured to provide a second output current at the output of the second amplifier circuit.

27. (Previously Presented) The circuit of Claim 26, further comprising:

a load circuit that is connected to the bus; and

a second current source circuit having at least an output, wherein the output of the second current source circuit is connected to the bus, and wherein the second current source circuit is arranged to provide a second local current at an output of the second current source circuit such that at least a portion of the second output current is prevented from being carried on the bus.

28. (Currently amended) A circuit for reducing the current density, comprising:

a first bus, a second bus, a third bus, and a fourth bus;

a first amplifier circuit that is arranged to provide a first differential current, wherein the amplifier circuit is arranged to provide a first half of the first differential current to the first bus, and to provide a second half of the first differential current to the second bus, wherein the first amplifier circuit has at least a first output that is coupled to the first bus and a second output that is coupled to the second bus;

a second amplifier circuit that is arranged to provide a second differential current, wherein the amplifier circuit is arranged to provide a first half of the second differential current to the first bus, and to provide a second half of the second differential current to the second bus, wherein the second amplifier circuit has at least a first output that is coupled to the first bus and a second output that is coupled to the second bus;

a third amplifier circuit that is arranged to provide a third differential current, wherein the amplifier circuit is arranged to provide a first half of the third differential current to the third bus, and to provide a second half of the third differential current to the fourth bus, wherein the third amplifier circuit has at least a first output that is coupled to the third bus and a second output that is coupled to the fourth bus;

a first current source circuit that is arranged to provide a first local current at the first output of the first amplifier circuit such that at least a portion of the first half of the first differential current is prevented from being carried on the first bus;

a second current source circuit that is arranged to provide a second local current at the second output of the first amplifier circuit such that at least a portion of the second half of the first differential current is prevented from being carried on the second ~~first~~ bus;

a third current source circuit that is arranged to provide a third local current at the first output of the third amplifier circuit such that at least a portion of the first half of the third differential current is prevented from being carried on the third bus; and

a fourth current source circuit that is arranged to provide a fourth local current at the second output of the fourth amplifier circuit such that at least a portion of the second half of the third differential current is prevented from being carried on the fourth bus.